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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/822,820	04/02/2001	Said El Fassi	P07156US00/RFH	8066

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STITES & HARBISON PLLC
1199 NORTH FAIRFAX STREET
SUITE 900
ALEXANDRIA, VA 22314

EXAMINER	
ZIA, SYED	
ART UNIT	**PAPER NUMBER**
2131	

DATE MAILED: 02/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/822,820	EL FASSI ET AL.	
	Examiner	Art Unit	
	Syed Zia	2131	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to request for reconsideration filed on December 08, 2005. Original application contained Claims 1-9. Applicant currently amended Claim 1. The amendment filed on December 08, 2005 have been entered and made of record. Therefore, Claims 1-9 are pending for consideration.

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on December 08, 2005 has been entered.

Response to Arguments

Applicant's arguments filed on December 08, 2005 have been fully considered but they are not persuasive because of the following reasons:

Regarding Claims 1-9 applicants argued that in cited prior art (CPA) [Veil et al. U. S. Patent No. 6,092,202] that, "*the security co-processor does not receive at least the input data codes, the operands, and the nature of the operation for each elementary operation performed by the main processor*," and cited prior art does not "*compute a code for each elementary operation performed by the processor" and verify proper operation of all or part of the executed program.*"

This is not found persuasive. Cited prior art clearly teaches system and method for where an interface interfaces a security coprocessor to a host computer. The interface includes the communication protocol for restricting access by the host computer to the data transmitted through the coprocessor. Secure transaction processing is performed locally in the security coprocessor and non-secure transaction processing is performed in the host computer. *The system of cited prior art compute codes for each elementary operation performed by the processor and verify proper operation of all or part of the executed program within the meaning of [sensitive data] that codes* (col.11 line 22 to line 44, and col.7 line 1 to line 49).

In the system of cited prior art (Fig.4, and 6) the data transmitted through the security coprocessor includes sensitive data such as personal and personal identification data. The interface communication protocol is implemented in application programming interface. A trusted input device such as keyboard and keypad is connected to the coprocessor. The input device includes a secure mode indicator for indicating secure mode in response to requests from host computer for keyboard entries of sensitive data. Thus, in the system of cited prior art the transactions are protected from unauthorized intrusion.

As a result, the system of cited prior art provides a system and method for a secure computer system as broadly claimed in system.

The examiner is not trying to teach the invention but is merely trying to interpret the claim language in its broadest and reasonable meaning. The examiner will not interpret to read narrowly the claim language to read exactly from the specification, but will interpret the claim language in the broadest reasonable interpretation in view of the specification. Therefore, the examiner asserts that cited prior art does teach or suggest the subject matter broadly recited in independent and dependent claims. Accordingly, rejections for Claims 1-9 are respectfully maintained.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Veil et al (U. S. Patent 6,092202).

1. Regarding Claim 1, Veil teach and describe a computer system (item 100 Fig.4) comprising at least one computer [PC 114] with a processor operating under the control of a program [such as operating system Unix, Windows of Fig.4 item102] (Col.1 line 26 to line 30), operating on input data items each suitable for being associated with a code [such as basic input/output code] and supplying output data items each suitable for being associated with a code

and for being transmitted or applied to output members [Basic I/P, O/P operation, using USB,PS/2 or RS-232 protocol to devices such as smart card item 46 Fig.4] (Col.10 line 54 to line 60), the system being characterized by at least one peripheral external to the processor [i.e. security processor item 122 Fig.4], connected to the processor receive at least the input data codes, the operands, and the nature of the operation for each elementary operation performed by the processor [input device with security circuit] (col.7 line 1 to line 15), the processor and the at least one peripheral [i.e. security processor item 122 Fig.4] both processing all types of said input data codes [such as basic input/output code], the peripheral having secure architecture [Item 104 Fig.4] and computing a code for each elementary operation performed by the processor and verifying proper operation of all or part of the executed program, while the processor performs computations only on the functional values [sensitive data] of the encoded [cryptographic] data (col.7 line 28 to line 49, and col.10 line 61 to col.11 line 8).

2. Claims 2-3, and 5-9 are rejected applied as above rejecting Claim 1. Furthermore, Veil teach ad describe a secure computers system and method (Fig.4, Fig.6) in which:

As to claim 2, the said program is permanent or downloaded (col.10 line 47 to line 54).

As to claim 3, the peripheral is single [item 102 Fig.4] and associated with a host computer [item 102 Fig.4] to provide security for all of a system having a plurality of computers connected to a common [item 134 Fig.4] communications medium (col.7 line 1 to line 7, col.7 line 29 to line 36).

As to claim 5, having a plurality of host computers [item 442 Fig.6], interconnected by a transmission medium [such as network 110 Fig.4] and each provided with a security peripheral (col.7 line 1 to line 51, and col.10 line 58 to col.11 line 8).

As to claim 6, the security peripheral or the security peripherals [item 104, 122 Fig.4] perform security operations only on the inputs/outputs of only some of the processors [item 442 Fig.6] (col.9 line 9 to line 15, and col.10 line 61 to line 68).

As to claim 7, having a single security peripheral [item 400 Fig.6], connected to a computation assembly constituted by a central unit processor [item 410 Fig.6] and peripherals [item 414, 416, 436, 438 Fig.6], said security peripheral having computation means (Fig.4) (col.10 line 34 to line 60) that perform: digital security processing [such as RISC based processing of security program] (col.10 line 34 to line 54); and security processing of the inputs/outputs (col.10 line 47 to line 60).

As to claim 8, characterized in that said security peripheral [item 400 Fig.6] is designed to make secure an assembly of the system constituted by a smart card [item 436 Fig.6], a reader [item 436, 414 Fig.6], and one or more computers involved in the processing [item 442 Fig.6], and constituting the system, and to generate the interchanges between the smart card [item 436 Fig.6] and the computers [item 442 Fig.6] (col.11 line 9 to line 44).

As to claim 9, the security peripheral is an ASIC [such as application specific hardware] (col.7 line 19 to line 28].

3. Claim 4 is rejected applied as above rejecting Claim 3. Furthermore, Veil teach ad describe a secure computers system and method (Fig.4, Fig.6) in which:

The host computer is fitted with a safety driver [item 120 Fig.4], which enables it to dialog with the peripheral and with the other computers (col.8 line 65 to col.9 line 15, and col.10 line 54 to line 60).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Syed Zia whose telephone number is 571-272-3798. The examiner can normally be reached on 9:00 to 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz Sheikh can be reached on 571-272-3795. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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February 12, 2006